UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte SANTANU DUTTA, and DEEPAK K. SINGH

Appeal 2006-2911
Application 10/005,551
Technology Center 2100

Decided: March 6, 2007

Before HOWARD B. BLANKENSHIP, MAHSHID D. SAADAT, and JEAN R. HOMERE, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellants have appealed to the Board from the Examiner's final rejection of claims 1-19.

We affirm-in-part.

BACKGROUND

Appellants' invention relates to an arithmetic-logic data processing circuit that seeks to efficiently execute "basic arithmetic operations" with binary operands. (Specification 1-3).

Independent claim 1 is illustrative of the invention:

> 1. A circuit arrangement for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M, comprising:
>
> an adder adapted to add representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout; and
>
> a multiplexer circuit coupled to the adder and adapted to output a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

The following references are relied on by the Examiner:

Daniels	4,203,157	May 13, 1980

Claims 1-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Daniels.[1]

[1] The Examiner has withdrawn the 35 U.S.C. § 112, second paragraph, rejection of claims 1-19 (Answer 3).

Rather than repeat the arguments, we make reference to the Briefs and the Answer for the respective positions of Appellants and the Examiner.

DISCUSSION

The Briefs and the Answer reveal that Appellants and the Examiner disagree on the proper construction of the term "multiplexer" and whether Daniels discloses "selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand."

A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. See *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Applied Digital Data Sys. Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test and identity of terminology is not required. *In re Bond*, 910 F.2d 831,834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). A patent examiner gives claims

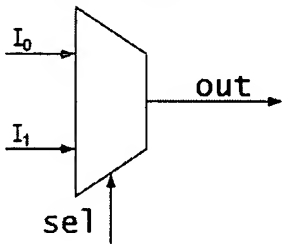
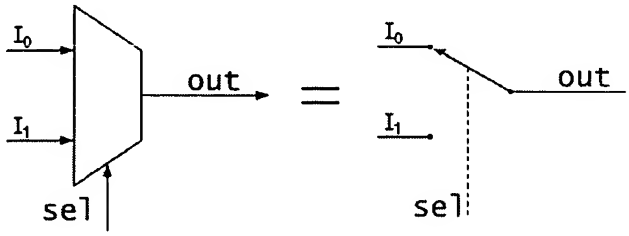
their broadest reasonable interpretation consistent with the specification. *See In re Morris*, 127 F.3d 1048, 1053, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

Although Appellants argue claims 1-19 as one group (Br. 8) under a single heading, we address each of the separate arguments with respect to: claim 1; claim 4, which depends from claim 3; claim 7, which depends from claims 5 and 6; and claims 11, 15 and 16, which each depend from claim 1. The Board of Patent Appeals and Interferences considers the patentability of each claim argued separately on appeal in light of the evidence of record. 37 C.F.R. § 41.37(c)(1)(vii), (ix).

A. Claim 1

Regarding the argued elements of claim 1, the main point of contention is whether Daniels discloses a multiplexer dependant on selection data that is a function of the most-significant bit of the representative set of least-significant bits of the first binary operand. Appellants characterize a multiplexer as a "device that has multiple input streams and only one output stream" and further state that "the cited portions of [Daniels] do not correspond to a multiplexer or multiplexer functionality." (Reply Br. 4). Both of Appellants' Briefs rely on a website, *www.wikipedia.com* (Wikipedia), arguing that the graphic in the left column below

represents a circuit element said to illustrate the function of a multiplexer. (Br. 7; Reply Br. 3). [2]

Graphic from Appellants' Brief	Graphic Displayed on Wikipedia
	

The right column of the complete reproduction of the Wikipedia figure as displayed on the Wikipedia website, shown above, reveals that Wikipedia equates a multiplexer to a switch that selectively enables one of multiple inputs to a single output.

Appellants' reliance on this definition in fact gives more support to the Examiner's argument (Answer 5), which encompasses the complete definition as shown in the Wikipedia graphic in the right column. We also find that the circuit in Daniels "enables either the output of INCH block 12" (the increment/decrement network, corresponding to I_0 in the graphic) "or the output of TEMPH register 16" (the temporary register, corresponding to I_1 in the graphic) "onto ABH bus 10" (the high-order address bus). (Daniels col.4, ll.47-54). Thus, the Wikipedia definition

[2] Appellants rely only on the left half of the drawing figure in Wikipedia in their Briefs.

of multiplexer fails to support Appellants' position that the selective enablement of one of two components to a common location in Daniels is different from the claimed multiplexer (Reply Br. 3). Similarly, the Wikipedia graphic fails to support Appellants' arguments that Daniels does not correspond to a multiplexer because the "the two possible outputs are located in two different locations," and that "there is no selection or control of the output of any signal at a multiplexer or other selection circuit because each of INCH 12 and TEMPH 16 is coupled directly to the bus ABH 10 (Br. 7; Reply Br. 3). Additionally, we also find that INCH 12 and TEMPH 16 in Daniels are both coupled to a single output location, ABH. (Daniels Figure 7). Therefore, Appellants' argument also fails to demonstrate how directly coupling INCH 12 and TEMPH 16 to the ABH bus precludes selection or control of the output.

Turning to the selection data, Appellants urge that the Examiner fails to identify in Daniels any selection data being "a function of the most-significant bit of the representative set of least-significant bits of the first binary operand" in a manner consistent with any claim rejections. (Br. 8). The Examiner responds (Answer 5) that Daniels' carry-out signal satisfies these criteria, citing the last sentence of the abstract, which states that both, "[t]he carry signal and the sign bit of the 8-bit operand control the mode of operation of the increment/decrement

network and determine whether the increment/decrement network or the temporary register will be selected to provide the most significant byte of the result." The Examiner further argues that Daniels' Figures 5 and 7 demonstrate that the output of the multiplexer in Daniels is a function of the carry-out. The carry-out signal affects the intermediate signal B7C in Figure 5, which, as shown in Figure 7, affects whether the increment/decrement network (INCH) or the temporary register (TEMPH) is output to the high-order address bus (ABH) (Answer 5).

Appellants further argue that the *sign bit* of the second binary operand does not qualify as proper selection data. (Reply Br. 5). Although Appellants' statement is factually correct, as stated by the Examiner (Answer 5), it does not apply to the carry-out signal. The output to ABH bus is a function of both the sign bit and the carry-out. (Daniels Abstract). Thus, whether or not the sign bit satisfies the selection data criteria, we are convinced by the Examiner's assertion that the carry-out signal constitutes the selection data.

We note that independent claims 18 and 19 recite similar limitations which, as discussed above, are taught by Daniels. Thus, we sustain the 35 U.S.C. § 102 rejection of independent claims 1, 18, and 19, as well as dependent claims 2, 3, 5, 6, 8-10, and 12-17 argued together as one group (Br. 8).

B. Claims 4, 7, 11, 15 and 16

Addressing the remaining rejections, Appellants argue that the Examiner fails to "assert or identify any correspondence between any of the dependent claims and [Daniels]," specifically arguing that none of claims 4, 7, 11, 15 and 16 receive proper rejection.[3]

With respect to claim 4, Appellants assert that Daniels lacks the limitation "wherein N is 24 and M is 16." (Br. 8). The Examiner argues that Daniels inherently includes this limitation "because Daniel speaks in terms of bytes, i.e. 8 bits, and his example is N being 16 and M being 8." (Answer 5).

Under the principles of inherency, if a structure in the prior art necessarily functions in accordance with the limitations of a process or method claim of an application, the claim is anticipated. *In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) (citing *In re Hack*, 245 F.2d 246, 248, 114 USPQ 161, 163 (CCPA 1957)). Furthermore, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the

[3] As permitted by 37 C.F.R. § 41.39, the Examiner responded with five new grounds of rejection, which are addressed below. Rather than opting to reopen prosecution after the Examiner's Answer, according to 37 C.F.R. § 41.39(2)(b)(1), Appellants maintained appeal, as permitted under 37 C.F.R. § 41.39(2)(b)(2), asserting as rebuttal that the Examiner's conclusions lack support in the record. Any questions or arguments related to the propriety of maintaining these rejections at this stage of prosecution are petitionable matters and will not be addressed by this panel.

thing described in the reference, and that it would be so recognized by person of ordinary skill.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-1951 (Fed. Cir. 1999) (citing *Continental Can Co. V. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991)). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result for a given set of circumstances is not sufficient." *Id.* 948 F.2d at 1268, 20 USPQ2d at 1749.

Applying these guidelines, we find that the Examiner has not pointed to, nor have we found, any teachings in Daniels showing that the claimed values for N and M are necessarily present in Daniels. Therefore, the 35 U.S.C. § 102 rejection of claim 4 cannot be sustained.

With respect to claim 7, Appellants argue that Daniels fails to teach the claimed requirement of "wherein the multiplexer circuit includes a multiplexer adapted to select one of at least three input binary quantities." Mistakenly identifying this limitation with claim 16, the Examiner argues that "Daniels does select one of at least three input binary quantities because Daniels increment/decrement network output[s] an incremented quantity and [a] decremented quantity and the temporary register outputs another quantity." (Answer 5-6).

Daniels discloses that, depending on the sign bit of the second binary operand, the increment/decrement network selects either "the increment or decrement mode" of operation for INCH block 12. (Daniels col. 4, ll. 66-68, col. 5, ll. 5-35). Subsequently, the multiplexer in Daniels, depending on the carry-out signal, enables either INCH block 12 or TEMPH onto ABH bus. (Daniels col. 5, ll. 47-58). As such, we find no support in Daniels for the Examiner's position and, therefore, do not sustain the 35 U.S.C. § 102 rejection of claim 7.

With respect to claim 11, Appellants argue that Daniels fails to teach "multiplexer circuit configured to operate as an exclusive-or gate." (Br. 8). The Examiner relies on Figure 4A of Daniels and characterizes elements 64, 67 and 69 as disclosing the claimed feature. However, the Examiner fails to explain how elements 64, 67, and 69 relate to the disclosed multiplexer operating as an exclusive-or gate, nor do we find any teachings in Daniels in support of such position. Accordingly, the 35 U.S.C. § 102 rejection of claim 11 cannot be sustained.

Turning now to claim 15, Appellants point out that Daniels fails to teach "wherein the operands are unsigned binary numbers." (Br. 8). The Examiner argues that the Daniels "system can operate on unsigned binary numbers."

(Answer 6). We find that Daniels clearly teaches this element. (Daniels, col. 4, l. 65 - col. 5, l. 5) and therefore, sustain the 35 U.S.C. § 102 rejection of claim 15.

Finally, with respect to claim 16, without relying on any part of the record, Appellants argue that the words "digital filtering circuit arrangement" constitute a limitation not taught by Daniels. The Examiner asserts that the alleged limitation merely recite intended use. Claim 16 explicitly recites a "digital filtering circuit arrangement, *according to claim 1*, ..." (emphasis added). Giving the claim the broadest reasonable interpretation, we find that the words "according to claim 1" qualify the previous clause "[a] digital filtering arrangement" only to the extent that the claim refers to the "circuit arrangement" in the preamble of claim 1 placing claim 16 in dependent form. Accordingly, since Daniels discloses the claimed features of claim 16, the 35 U.S.C. § 102 rejection of claim 16 is also sustained.

CONCLUSION

In view of the foregoing, the Examiner's decision rejecting claims 1-3, 5, 6, 8-10, and 12-19 is affirmed, but is reversed with respect to the rejection of claims 4, 7, and 11.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R .§ 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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